Research on Fault-Tolerant Technology of Embedded Computer Control System

Honghui Lai¹, Rong Wang², Hua Liao³

¹ College of Information Engineering, Gannan Medical University, Ganzhou, 341000, China

Keywords: Fault-Tolerant Technology; Embedded Computer Control System; Redundancy Method

Abstract. With the rapid improvement of the computer control system, the fault-tolerant computer control technology has been applied into many fields. Based on this actual background, the fault-tolerant technology of embedded computer control system is studied in this study, to improve the reliability of present computer system and guarantee the stability of system operation. To find out main system faults, the structure of computer fault-tolerance control system is presented at first, based on which the principal method to achieve the fault tolerance control system is derived. Finally, three principal redundancy methods to achieve the fault tolerance control system are provided, which can be helpful to improving the reliability and stability of the computer system operation

Introduction

With the rapid improvement of the computer control system, the fault-tolerant computer control technology has been applied into many fields such as space navigation, aviation, process control, engineering design, management, military and so on, which is expected to reduce the possibility of security incidents caused by the computer system failure and improve the reliability of the embedded computer control system [1]. As a result, it is necessary to study the embedd computer control system thoroughly, to find out the most frequent errors and develop pertinent measures [2]. This study on the fault-tolerant technology of embedded computer control system is helpful to improve the reliability of present computer systemn and guarantee the stability of system operation.

In general, the system containing programmable computer controller is called the embbed computer system, which has been widely used in many fields. Based on the relevant data provided by Tanaka Y [3], the embedded computer systema are applied into nearly 99.9% of annual production of CPU (Central Processing Unit). However, there are some softwares implaned into the ROM (Read Only Memory) of the embbed computer systems before coming into service, which makes the hardwares and softwars of different computer products have great difference [4]. As a result, the embbed computer softwares are usually difficult to modify. Based on this consideration, the falut-tolerant stategy is adopted to improve the flexibility of the embedded computer control system, whihe can be helpful to developing efficient measures according to different faults and errors, to make the computer systems operate more stabaly and safely [5].

Embedded computer control system fault-tolerant design includes all kinds of methods that can reduce the effect of system faults, including fault detect and diagnose (FDD), dependable hardware technique, dependable software technique and so on [6]. The control system operation needs correct sensor data, while the incorrect data are usually caused by some disturbances or sensor faults. As a result, the fault-tolerant softwares are extremely important to implement the computer control system with high reliability, based on which a series of method can be applied to avoid system disturbances and implement fault tolerance, such as instruction redudancy, software redudancy, software trap, software watch timer dog and so on [7]. On the basis of module technique, the embedded software reconfiguration can be achieved easily, including recovery block, N-version and software injection and so on. As usual, the validity of the fault tolerance needs to be verified, and a method of injecting software and hardware errors to verify the power control system fault tolerance was presented by

² College of Information Engineering, Gannan Medical University, Ganzhou, 341000, China

³ STATE GRID GANZHOU ELECTRIC POWER SUPPLY COMPANY, Ganzhou, 341000, China

Goswami D et.al. [8]. In the study, the fault analysis tree needs to be built at first, then the fault mode is analyzed to produce all faults generated by simulators and emulators to verify the fault-tolerance.

In this study, the structure of computer fault-tolerance control system is presented at first, based on which various types of system faults are analyzed. Secondly, the principal method to achieve the fault tolerance control system is provided, which is based on the concept of redundancy. The proposed redundancy methods can be combined with the practical computer control system structure to improve the reliability and stability of the computer system operation.

Computer Control System Structure

The computer control system structure is the basis to analyze the types if common systematic faults, which can be divided into two parts: hardware composition and software composition.

Hardware Composition. The computer hardware composition block diagram is shown in Fig.1, which mainly contains five components: control hostcmputer, peripheral equipments, input and output channel, interface circuit and operating platform [9].

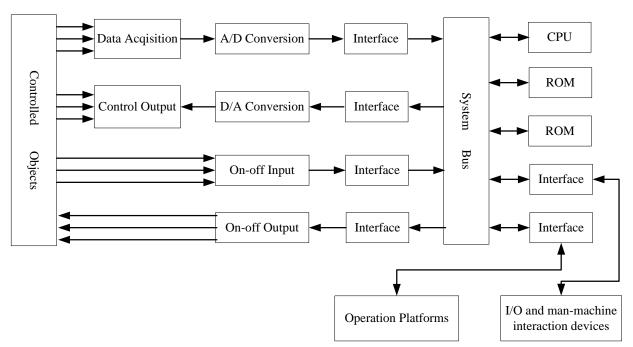


Fig.1. The computer hardware composition block diagram

Software Composition. The common control system softwares include operation system, monitoring program, program language, compile program, checking program and application program [10]. In the computer control system, each controlled object or controlling task needs to be equipped with corresponding control programs, which are used to satisfy different requirements of controlled objects.

As far as the systematic function concerned, the computer programs can be classified as the front-end program, service program and back-end program. The front-end programs are usually related to the controlling process, which can guarantee that the system can complete the fundamental tasks [11]. The service programs make the computers control all peripheral equipments and achieve man-machine interface, whihe are usually called monitoring programms. The back-end programs have no connection with the controlling process, whihe are only to make the system operate stably.

Operating Mode of the Fault Tolerance System

The fault tolerance is referred to the ability that the computer operation system would not lose data and the present working progress would not be damaged once systematic faults (such as power failure, hardware fault and other unexpected conditions) occur, which can be achieved by many precautionary measures including back-up power, back-up hardwares and some prevention mechanism implanted in softwares [12]. The computer system fault tolerance design is a kind of specific design method to cope with some disastrous systematic faults, including systematic fault monitoring and diagnosis, hardware and software reliability design. For the real-time control system, the fault tolerance design is expected to meet the features of control system, including monitoring and diagnosing controlled objects plus actuators, control system degraded running under the condition of unrecoverable hardwares and lacking redundant backup.

The fault tolerance design is based on the redundancy design method that can provide the information to eliminate the failure effect, and there are mainly two ways to achieve the redundancy: extra time (time redundancy) and extra functional unit (function redundancy). The time redundancy is achieved by performing the same calculation to compare multiple calculated results to provide basis for the next operation, which is usually achieved by softwares. The function redundancy is achieved by extra gates, storage components, bus and functional modules. Based on the different failure conditions, the fault tolerance system design includes many steps, such as fault restriction, fault shielding, retry, diagnosis, recombination, restarting, repairing and reconstruction.

Redundancy Fault Tolerance Method

In this section, three redundancy fault tolerance methods are presented, which are expected to improve the reliability and stability of the present embedded computer control system.

Redundancy Design on Circuit Level. The electronic circuit faults are mainly caused by the components failure, and therefore redundancy technology applied into the circuit level can be used to obtain better shielding effect. The basic components in the electronic circuit are diode and triode, which usually serve as the switching element with main faults of short circuit and open circuit. The quadruple redundancy triode circuit assembled in two ways are presented as follows: series connection first and prallel connection next; prallel connection first and series connection next

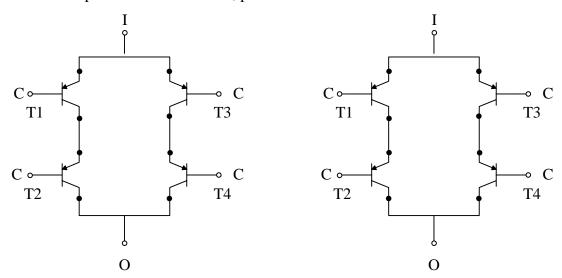


Fig.2. Two kinds of quadruple redundancy triode circuits

Static Redundancy System. The static redundancy structure would not change with the fault conditions variation, where the fault shielding concept is used to hide the existing faults. The basic principle of the static redundancy is to mask the current faults by multiple votersm, of which redundancy module is one part of overall system. In terms of static redundancy module, multiple modules would perform same functions, and the output is the majority consensus generated by the

voters. The most commonly used static redundacny is the triple modular redundancy (TMR), whihe is shown in Fig.3.

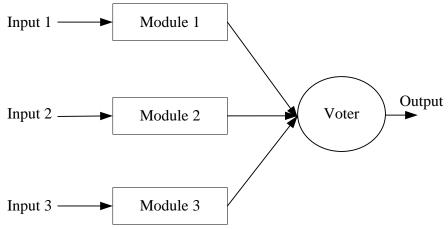


Fig.3. Triple modular redundancy struture

Dynamic Redundancy System. The typical structure of the dynamic redundancy system is shown in Fig. 4, which has N+1 same modules and only one module would be in running state while other N modules are in backup state.

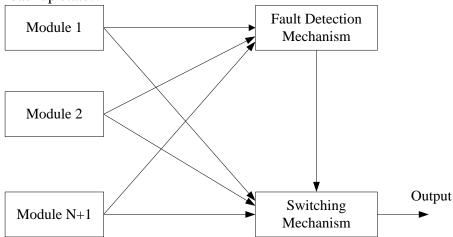


Fig.4. Dynamic redundancy system struture

Summary

The fault-tolerant computer control technology has been applied into many fields, to reduce the possibility of security incidents caused by the computer system failure and improve the reliability of the embedded computer control system. As a result, it is necessary to study the embbed computer control system thoroughly, to find out the most frequent errors and develop pertinent measures. Based on this background, this study focuses on fault-tolerant technology of embedded computer control system, which is helpful to improve the reliability of present computer systemn and guarantee the stability of system operation. Based on the definition of fault tolerance, the structure of computer fault-tolerance control system is presented at first. Secondly, the principal method to achieve the fault tolerance control system is provided, which is based on the concept of redundancy. The proposed redundancy methods can be combined with the practical computer control system structure to improve the reliability and stability of the computer system operation.

References

- [1] Sun W T, Girault A, Delaval G. A formal approach for the synthesis and implementation of fault-tolerant industrial embedded systems[C]// IEEE International Symposium on Industrial Embedded Systems. IEEE, 2015:1-9.Lemons J F. Issue: Flat Management Short Article: Consulting Firm Experiments with 'Holacracy' [J]. 2017.
- [2] Khadse T S, Karmore S P. A Novel Approach for Fault Tolerance Control System and Embedded System Security [J]. Procedia Computer Science, 2016, 78:799-806.
- [3] Tanaka Y. Fault-tolerant computer system, fault-tolerant computer system control method and recording medium storing control program for fault-tolerant computer system: US, US 8990617 B2[P]. 2015.
- [4] Goswami D, Müller-Gritschneder D, Basten T, et al. Fault-tolerant embedded control systems for unreliable hardware [C]// International Symposium on Integrated Circuits. IEEE, 2015:464-467.
- [5] Moorthy S. An Introduction to Fault-Tolerant Embedded Systems[J]. Electronics for You, 2015.
- [6] Gao M. An Embedded ARM Fault-Tolerant Control System Based on Structure of Hot Standby[J]. Computer Measurement & Control, 2013.
- [7] Goswami D. Fault-tolerant control synthesis and verification of distributed embedded systems[J]. 2014.
- [8] Goswami D, Muller-Gritschneder D, Basten T, et al. Fault-tolerant embedded control systems for unreliable hardware[J]. IEEE Service Center, 2014.
- [9] Ibrahim M, Asami K, Cho M. Fault Tolerant Architecture Alternatives for Developing Nano-Satellites Embedded Computers[C]// AIAA SPACE 2012 Conference & Exposition. 2013.
- [10] Yoo J, Han K. The Design of Fault Tolerant PSTR Using Virtualization Techniques on the Embedded System[J]. Kips Transactions on Computer & Communication Systems, 2014, 3(12):443-448.
- [11] Neela A G, Prabhu S S, Baligar C. Fault Tolerant Operation in Aero Engine Using Distributed Computation System[J]. International Journal of Technological Exploration & Learning, 2014, 3(2).
- [12] Sourdis I. Special session on "Fault-tolerant techniques for computer systems, architectures and processors" [C]// International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation. 2013:245-245.